Offshoring in the Semiconductor Industry:

A Historical Perspective

Clair Brown and Greg Linden
U.C. Berkeley

Abstract:

Semiconductor design is one of the many white-collar job categories considered to be at risk from offshoring by U.S. companies via investments and outsourcing. Data about this activity are scarce and hard to interpret, but there is much to be learned from looking at earlier periods in the industry's history when other phases of the semiconductor value chain – assembly and fabrication – experienced rapid offshore expansion.

This paper reviews the lessons from these earlier offshore movements of semiconductor industry jobs. Then it analyzes the current experience of the offshoring of semiconductor design based on our ongoing field research.

The experience of earlier periods supports the claim by some that offshoring is a reasonable response to the competitive challenges and opportunities facing the semiconductor industry, and that the industry will adapt in ways that aren't necessarily clear from the outset. Nevertheless, there is evidence that some U.S. chip design engineers face at least short-term displacement as a result of the industry's current round of globalization.

October 7, 2005

This is a work-in-progress with data collection still underways. An earlier version was presented at the 2005 Brookings Trade Forum on Offshoring of White-Collar Work. A revised version will be available earlier next year in the Trade Forum proceedings.

Acknowledgments

The authors would like to thank the Alfred P. Sloan Foundation, the Institute for Technology, Enterprise and Competitiveness (ITEC/COE), and Omron Fellowship at Doshisha University for funding, and the Institute of Industrial Relations, UC Berkeley, for administrative support. We are grateful to Koji Ban, Ben Campbell, Michael Flynn, Ron Hira, Dave Hodges, Rob Leachman, Elena Obukhova, Devadas Pillai, Amy Shuen, Gary Smith, Strategic Marketing Associates (www.scfab.com), and Bill Van Der Vort for their valuable contributions to this paper. We would also like to thank Jeff Macher for his detailed and helpful comments, and Melissa Appleyard, Hank Chesbrough, Jason Dedrick, Rafiq Dossani, Richard Freeman, Deepak Gupta, Bradford Jensen, Ken Kraemer, Frank Levy Tim Sturgeon, Eiichi Yamaguchi, and participants at the 2005 Brookings Trade Forum on Offshoring of White-Collar Work and the Doshisha ITEC seminar series for thoughtful discussions, which improved the paper The authors are responsible for any errors.

Semiconductor design is a frequently-cited example of the new wave of offshoring of service sector jobs.[1] It is certainly a concern to U.S. design engineers themselves.[2]

The semiconductor industry already has a rich experience with the offshoring of manufacturing activity. Semiconductor (or chip) companies were among the first to invest in offshore facilities to manufacture goods for imports back to the U.S. A review of these earlier manufacturing experiences and their impact on the fortunes of the domestic industry and its workers can help to illuminate the current debates over the offshoring of services.

Because meaningful data about the impact of the offshoring of chip design (and even of manufacturing) are limited, we rely on a more qualitative analysis for our key points. We have conducted dozens of interviews with engineers and managers at numerous semiconductor and related companies in the United States, Asia, and Europe over the past twelve years. Our research also incorporates the rich store of publicly-available information in trade journals and company reports.

Before addressing semiconductor design directly, we begin by analyzing the impact on the U.S. semiconductor industry of the offshoring of semiconductor assembly and fabrication. We argue that the initial concern about losing domestic jobs in both stages turned out to be unfounded as the industry used the situation to its competitive advantage by becoming cost competitive (through assembly offshoring) and by developing the fabless sector (through foreign outsourcing of chip fabrication or manufacturing). We then analyze the ongoing offshoring of design jobs, and compare this stage to the two that came before in order to explore the possible impact on domestic jobs and the U.S. semiconductor industry.

The paper begins in section one with a brief description of the stages of semiconductor production and our analytical framework. Section two looks at the offshoring of assembly jobs, and section three analyzes the offshoring of manufacturing. Section four explores the offshoring of design jobs, and concludes with a discussion of what this means for the U.S.

I. Introduction: The Industry and Analytical Framework

In order to understand the offshoring of activities in the semiconductor industry, we begin by describing the stages of production.

The most important type of semiconductor, and the one on which this study is focused, is the integrated circuit, or "chip," which is basically a network of tiny wires fabricated on a surface connecting transistors that switch on and off for processing data in binary code.[3] The development and manufacturing of chips involve three primary activities in the value chain: design, fabrication, test and assembly. The semiconductor industry has successively undergone the offshoring of each of these activities—first assembly, then fabrication, and now design.

During design, the desired electronic circuits progress through a series of abstract representations of increasing detail. During fabrication, the circuits of the chips are built up on the surface of a flat, round silicon wafer in successive layers Assembly is, typically, the process of cutting the wafer into individual chips (or die), which can number in the thousands, depending on die size, and packaging the delicate chip in a protective shell that includes connections to other components.

The economic characteristics of each step of the process differ significantly. Design is skill intensive, and requires expensive EDA (electronic design automation) software, which is typically licensed per design engineer. Fabrication requires a huge fixed investment (currently on

[1] See for example "The New Global Job Shift," Business Week, February 3, 2003, cover story and "Another Lure Of Outsourcing: Job Expertise," Wall Street Journal, April 12, 2004, p. B1.

[2] "2004 Salary Survey: It's an outsourced world, EEs acknowledge," EE Times, August 27, 2004.

[3] Other types of semiconductors, such as single transistors or diodes, use different design and manufacturing methods not subject to the same economic forces discussed in this paper. These other categories constituted about 15% of the total semiconductor market in 2004 ("WSTS Semiconductor Market Forecast," World Semiconductor Trade Statistics press release dated November 2, 2004.).

the order of $2 billion) to build a plant (called a fab) that holds a wide variety of expensive equipment and that meets extreme requirements of cleanliness. Assembly also requires expensive equipment, but the overall costs of plant and equipment are much lower than for the fab, as are the average skill requirements. Overall, worker skill requirements go down along the value chain (i.e., design is more skill-intensive than manufacturing, which is more skill-intensive than assembly).

However, equipment costs dominate labor costs, especially for fabrication, and this has limited the attractiveness of low-cost labor locations. Even the most labor-intensive activity, chip assembly, has become more automated over time. As discussed below, other costs, including those relating to land, taxes, and government regulations, often affect decisions to invest offshore.

The framework for this analysis of the offshoring of the stages of the industry value chain relies on the concept of competitive advantage, which is linked to offshore investing and outsourcing, and, ultimately, to domestic jobs.[4] A sustained advantage over rivals can be built on product (i.e., the intellectual property that defines functionality), price (i.e., the cost of production), or market attributes (i.e., new customers, customer service, brand reputation, and links to legacy products). These sources of competitive advantage correspond to the three principal reasons that firms globalize their activities: access to location-specific resources including engineering talent, cost reduction, and market development.

When a firm with some non-imitable advantage moves an activity offshore to reduce its costs or improve access to resources or markets, it improves (barring cases where the move is mismanaged) its competitive position against its rivals. In an expanding market like that for chips, the firm will grow and will hire more workers, some of whom will be in the home country and some offshore.

However, some or all of the workers in the home country who were engaged in the activity that shifted offshore may lose their jobs, so that only the remaining home country workers benefit from the firm's move offshore, along with the consumers of the lower-price products.[5] In addition, exports and imports are increasing with market growth, which clouds the impact of offshoring on jobs.[6]

In the longer term, numerous firm-level investments in a foreign location may transform the location in such a way that it presents a new set of opportunities that lead to a transformation of the industry. A foreign location that is initially little more than a source of lower costs, especially labor, might develop over time as a specialized supply base, particularly in the presence of incentives and infrastructure provided by the host country government. The changes can increase the value of the location to the point that the industry eventually restructures around the new distribution of skills such that offshoring becomes the preferred mode for this part of the value chain. It will be discussed below how this occurred for semiconductor assembly, but it has also taken place in other industries, such as hard disk drives.[7]

In other words, the pursuit of offshoring to gain competitive advantage in the context of a growing market initiated a dynamic process that has made the net employment effect difficult to estimate even after the fact. Table 1 summarizes our analysis of the three segments of the semiconductor value chain that is presented in the following sections of the paper.

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[4] Porter (1985).
[5] See, for example, Garner (2004) for further discussion.
[6] Groshen, Hobijn, and McConnell (2005).
[7] McKendrick, Doner, and Haggard (2000).

Table 1: Summary of Facts and Findings by Industry Segment

Value chain segment	Assembly	Fabrication	Design
Share of engineers in workforce of the segment	6%	24%	85%
Key economic characteristics	Moderately capital-intensive; requires access to low-cost direct labor	Highly capital-intensive; requires access to infrastructure and experienced process engineers	Highly skill-intensive; requires access to experienced designers and end users
U.S. experience with offshore investments	Shifted to developing countries beginning in 1960s	Cross-investments with other developed countries beginning in 1970s	Offshore investments to both high- and low-wage countries beginning in the 1980s
Impact on the U.S. industry	Offshoring helped U.S. firms respond to the initial Asian competitive threat at cost of "hollowing out" the domestic assembly sector	Offshoring by U.S. firms has been largely offset by foreign investments in the U.S.	Offshoring has entered a period of expansion while domestic employment was flat during the period of slow growth.
US experience with foreign outsourcing	Asian outsourcing started in late 1960s	Asian outsourcing started in mid-1980s	Asian outsourcing started in the 1990s
Impact on the U.S. industry	Outsourcing helps U.S. firms reduce their investment in capacity and in the variety of chip packages.	Outsourcing stimulated the emergence of a "fabless" chip sector and helps fab-owning firms reduce their risk of overcapacity.	Long-term result uncertain. May have curbed domestic hiring but allows start-ups to compete.

SOURCE: Points from the text

II. Assembly: from in-house offshoring to offshored outsourcing

Assembly was the easiest stage of production to move offshore. It was functionally separate from the other stages of production even when performed in close proximity to fabrication. Furthermore, assembly began with a relatively high use of less-skilled direct labor, making it an attractive target for cost-reduction offshoring.

During the 1980s, the U.S. offshore chip assembly subsidiaries switched to automation in response to a combination of increasingly intricate packaging requirements beyond the skills of manual labor along with rising wages in some South-East Asian nations. A typical chip assembly plant employs 1,000 or more workers. As of the mid-1990s, low-skilled workers made up about 80% of the staff of offshore assembly plants. The share of engineering and professional jobs was about 6%, and technicians made up another 13%.[8]

[8] The Advanced Micro Devices chip assembly subsidiary in Penang, Malaysia employed 160 engineers and 380 technicians out of 2,900 workers ("Firm to make new microchips," The Star, May 25, 1996). This ratio is similar to that

The move to offshore assembly led to a "hollowing out" of the U.S. chip assembly sector, but kept the U.S. chip industry cost-competitive as new rivals appeared in Europe and Japan. Over time, Asian suppliers appeared and are taking over a growing portion of the assembly business, so it went from in-house offshoring to offshored outsourcing. Most large chip companies still own assembly plants in Asia.

The main lesson from this period of offshoring is that giving up one part of the value chain (at least as far as domestic production is concerned) may help to "save" the domestic industry.[9] The second lesson is that the initial moves offshore can have unforeseen dynamic consequences such as the emergence of foreign suppliers who dominate the industry segment.

A. Offshoring, job loss, and competition

Because of their high value-to-weight ratio, semiconductors could profitably be fabricated in the United States, air-freighted to Asia for assembly, and then returned to the United States for final testing and shipment to the customer. This system allowed the U.S. companies to take advantage of the specialized skilled and semi-skilled labor in the United States for design, fabrication, and key managerial functions while tapping the lower cost unskilled labor, land, and taxes of Asia for assembly. Today, the trans-oceanic division of labor between fabrication and assembly still takes place. Final testing was added to Asian assembly plants in the 1980s, which allows the finished chips to be shipped directly to customers from Asia, which is where a large share of the market is also located. From 1984 to 2004, the share of semiconductor sales in Asia, including Japan, has risen from 38 to 63% of the world total.[10]

The earliest offshore investment in semiconductor assembly was made in 1961 by Fairchild Semiconductor in Hong Kong for the assembly of discrete transistors. Over the next fifteen years, this pioneering investment was followed by assembly investments by other companies in seven other economies of the region. By the mid-1970s, there were dozens of U.S.-owned assembly plants throughout the region employing about 1,000 workers each.[11]

Developing economies in the Western hemisphere such as Mexico and El Salvador received assembly investments, but during the 1970s gradually receded from one-quarter to one-tenth of U.S. re-imports in the face of political or social unrest, while East Asia made up the difference.[12] The Asian countries offered plentiful low-skilled workers and stable governments that adopted pro-investment policies.

All large U.S. "merchant" (selling to other companies) chip firms invested in offshore assembly. The two primary "captive" (for internal use) producers, IBM and AT&T, initially kept their assembly in the United States and adopted a higher level of automation than the offshore plants.[13] For at least one U.S. company, Philco, an attempt to automate in the U.S. ended badly because of the rapid obsolescence of the equipment.[14] AT&T opened chip assembly plants in Singapore and Thailand in 1985. IBM announced a large chip assembly investment in China in 2000, but ended up selling that operation plus a testing facility in Singapore to Amkor, a major Korea-based assembly subcontractor, in 2004 as part of a plan to move from in-house offshore to 100%-outsourced assembly.[15]

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for the whole semiconductor-dominated Malaysian-American Electronic Industry group in 1994 as reported in their Annual Survey of 17 members over the preceding five years (MAEI, 1995).

[9] A complete analysis of the connection between the offshoring of assembly and industry competitiveness is beyond the scope of this paper. The move provided short-term breathing space for U.S. firms facing low-cost competition. This is not to say that other strategies might not have provided equal or better results.

[10] Calculated from Semiconductor Industry Association market statistics available at www.sia-online.org/pre_statistics.cfm.

[11] Henderson (1989, p. 51).

[12] Flamm (1985, Table 3-7).

[13] Flamm (1985, p. 52).

[14] ibid. (p. 69).

[15] "IBM jettisons IC-packaging units, sells plants to Amkor," Silicon Strategies, May 18, 2004.

Several factors contributed to the movement of assembly offshore. First, Japanese manufacturers, who automated their assembly lines, provided stiff competition for American producers.[16] Automation was a more feasible strategy for the Japanese because of their relatively greater reliance on high-volume memory chips, which involve long production runs. U.S. companies produced a wider range of products which were less economical to automate.[17] Also, the military, which had been the primary early adopter of semiconductors, was steadily replaced by the consumer electronics industry, with its attendant price pressures, during the 1960s.[18] Furthermore, U.S. policy was permissive because tariffs were limited to the value added offshore, which in the case of assembly was a relatively small portion of the total – about 12% in the late 1970s.[19]

By 1977, U.S. companies employed close to 100,000 workers in offshore assembly plants, compared to 114,000 domestic employees, of whom 64,000 were directly involved in production.[20] The overseas expansion resulted in a decline in domestic assembly jobs. U.S. factories were closed during recessions, and new jobs added overseas during upturns. Job-loss data from the period of peak overseas expansion (1968-1972) aren't available; but from 1975 to 1982, 8,500 former chip assembly workers were certified for trade-adjustment assistance, and another 3,000 applied but were refused.[21]

There was, however, an offsetting gain in consumer surplus from the low prices of the re-imported chips. Flamm (1985) estimates the welfare cost of repatriating assembly and making it profitable with tariff barriers to be about $1 billion for 1983, which can be thought of as an upper bound for the consumer surplus created by the move offshore.[22]

In terms of assembly, the U.S. chip industry "hollowed out." Flamm (1985) estimated that in 1978 around 80% of U.S. semiconductor production was assembled abroad.[23] The figure is now probably above 95%, with most remaining U.S. facilities predominantly engaged in prototyping and military jobs. This implies U.S. firms are doing around 60% of assembly in offshore subsidiaries.

History suggests that the move offshore helped keep U.S. chip firms competitive with the new rivals from Asia, and this was important for protecting the remaining jobs in the industry. When Flamm published his landmark study, the U.S. chip industry was in a period of decline, but in spite of the move to offshore assembly rather than because of it. When the industry sought U.S. government help, the fabrication stage of production was where the U.S. capability was seen as deficient, and fabrication was the focus of the joint public-private research consortium, SEMATECH, launched in 1986.

Thus chip assembly provides an example where the offshoring of one part of the value chain to reduce costs was important for maintaining overall cost competitiveness against international rivals, albeit at the expense of specific (primarily low-skilled) jobs in the short run.

B. The appearance of new suppliers

Offshore chip assembly offers an additional lesson that is worth noting briefly, namely that in-house offshoring can generate technology diffusion to foreign companies.

In countries where entrepreneurial conditions are favorable, foreign investment stimulates the emergence of local companies, often started by ex-employees of the foreign company, that offer low-end versions of the foreign company's technology. In the case of chip assembly, this

[16] Henderson (1989, p. 45).
[17] Flamm (1985, p. 92).
[18] Henderson (1989, p. 43).
[19] Flamm (1985, Table 3-10).
[20] ibid. (p. 91).
[21] ibid. (p. 96).
[22] Flamm (1985, p. 96).
[23] Flamm (1985, p. 82).

has meant the emergence of a number of contract assemblers that complement, and arguably strengthen, the U.S. semiconductor industry. With Asian suppliers covering more mature technologies, the foreign subsidiaries are able to specialize in higher-value types of chip packaging.

Beginning in the late 1960s, local Asian firms started offering contract chip assembly services to the U.S.-owned plants. Today, roughly one third of all chip assembly is foreign outsourced, and the figure has been growing rapidly in recent years as the complexity and diversity of packages has increased.[24] The top 10 assembly contractors, with about 70% of total contracting revenue in 2003, are all Asia-based, which reflects a strong link to the initial locational choices of U.S. firms.[25]

The Asia-based outsourcing providers have become more technologically sophisticated and can serve as important technology partners for U.S. producers.[26] The requirements for chip packages have become quite challenging with the growing complexity of chips, the need to fit into size-sensitive products like mobile phones, and an increasing danger of package-induced electrical problems. The engineers at the leading Asian assembly companies are able to participate with the chip designers at an early stage to avoid problems with the final product.[27] The availability of multiple Asian suppliers allows chip companies access to the large array of package types that are now available, since few U.S. firms have the scale to supply internally all types that they need. The availability of assembly services is also vital to the growing group of design-specialist "fabless" firms, which will be discussed in the next section.

The entry of companies from industrializing economies into the chip assembly business has not brought about the exit of U.S. companies from the activity. Many U.S.-owned offshore assembly plants from the industry's early days are still in operation, and new ones are still being built, such as Intel's assembly plants in China.[28] The main reasons for keeping assembly in-house are technological, because electrical interaction between the packaging and the circuitry (a growing problem as the circuits shrink) can affect performance and reliability. There is also a strategic aspect of avoiding over-dependence on an assembly contractor. Furthermore, outsourced test (often provided with assembly) exposes some of the chip's embedded intellectual property. So the chips most likely to be outsourced by the major chip firms are low-end or otherwise mature chips where electrical interference and intellectual property are less of a concern. Chip makers also use outsourcing providers for buffer capacity in the case of excess demand and to handle specialized packages for low-volume products, for which the outsourcing provider may achieve better scale economies by aggregating across multiple customers.

III. Offshore Fabrication: from foreign outsourcing to industry restructuring

The case of wafer fabrication is very different from that of assembly because offshore investments were made, beginning in the 1970s, primarily for market access in Japan and Europe, where trade barriers made U.S. exports uneconomical, rather than to lower production costs.[29]

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[24] Amkor estimates that 32% of assembly and test activity was outsourced in 2004 (reported in Amkor's first quarter 2005 corporate presentation, accessed June 9, 2005 at www.amkor.com/IR/AMKR_Investor_presentation.pdf). This is up from about 20% in 2002 (Amkor estimate reported in "Amkor: A Promising Play in Chips," BusinessWeek Online, January 10, 2003).

[25] "Outsourced Semiconductor Assembly and Test: Preparing for the Next Boom Cycle, 2006-2008," Chip Scale Review, April 2005.

[26] One of the largest assembly providers, Amkor Technology, was founded in South Korea in 1968 and technically became a US-based firm through an Initial Public Offering in 1998 during the Asian Financial Crisis, although control of the company did not change.

[27] See "How Amkor's packaging proficiency helped Cisco's switches," Electronics Design Chain, Fall 2004, for a detailed case study.

[28] "Intel to build second IC assembly plant in Chengdu," EE Times, March 23, 2005.

[29] Henderson (1989, p. 45).

The employment impact of these market-seeking investments was to some extent offset by the cross-investments of European and Japanese producers in the United States. Cost reduction via offshore investments in low-wage countries was not a feasible strategy because fabrication is so capital-intensive that labor typically accounts for 16% of costs (including depreciation) in U.S. fabs producing 200mm wafers, and less than 10% in the newer 300mm fabs, which undercuts the major labor cost advantage of most industrializing countries.[30]

In a survey of industry executives, Leachman and Leachman (2004) found that the top five reasons, rated very close together, for fab site selection were "Tax advantages," "Supply of engineering and technical talent," "Quality of water supply and reliability of utilities," "Proximity to existing company facilities," and "Environmental permitting process and/or other regulations."[31] Empirical research on fab investment data shows that host country political institutions, the presence of other fabs, and a firm's prior investment experience also affect the location of fab investments.[32] This multiplicity of concerns surrounding such a major investment accounts for the relatively few cases of U.S.-built fabs in industrializing countries, even with the rich subsidies that have been offered by countries like Singapore.

Despite the limited occurrence of fab investment in industrializing countries, some of them, especially Taiwan, have successfully fostered local chip fabrication with focused government programs. The most successful business model for these fabs is contract fabrication for chips designed elsewhere, and this outsourcing model is discussed in the next section.

A. Foreign outsourced fabrication

The foreign outsourced fabrication of U.S.-designed chips to suppliers based mainly in Asia is a growth industry. These suppliers, known in the industry as "foundries," manufacture chips to the designs of other companies and sell no chips of their own design. Although some integrated companies, most notably IBM, offer foundry services, the "pure-play" companies are the most important source of such services to the rapidly-growing design-only ("fabless") sector.

The foundry-fabless business model, which emerged in the mid-1980s, was initially ridiculed by industry executives, most famously by Jerry Sanders, then-CEO of Advanced Micro Devices, who is reputed to have dismissed the phenomenon of outsourced fabrication with the claim that "Real men have fabs."[33] The foundry model has, however, proved to be extremely successful, and the technology level of the leading foundries is now close to the industry "bleeding edge" of companies such as Intel and IBM.[34]

The dedicated foundry model originated in Taiwan in 1987, when the government brought together investors, licensed mature production technology from the United States, and attracted Taiwanese engineers and managers with experience in the U.S. chip industry. The initial foundry, Taiwan Semiconductor Manufacturing Corporation (TSMC), remains the largest in an increasingly crowded field, as shown in Table 2. TSMC was founded by Morris Chang, a Chinese-born, MIT-educated executive with 25 years' experience at Texas Instruments who moved to Taiwan in 1985.

At the time TSMC was created, a handful of U.S. chip companies, such as Xilinx and Chips & Technologies, were already outsourcing all of their manufacturing, primarily to

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[30] Authors' calculations based on data in Appendix 2 of Howell and others (2003). Labor costs for 200mm fabs are 8% in Taiwan and 3% in China.

[31] Leachman and Leachman (2004, p. 226).

[32] Henisz and Macher (2004).

[33] Although the phrase is universally attributed to Mr. Sanders, the exact date and wording is obscure.

[34] "Have the foundries caught up?" Electronic Business, June 2005. Companies at the industry's "bleeding edge" are the first to put a new technology generation into production, which forces them to bear a relatively large burden of learning costs in exchange for potential first-mover advantages. Follower firms benefit from spillover knowledge flows. See Ham, Linden, and Appleyard (1998, p. 140) for an example of the adoption of new wafer sizes.

integrated Japanese manufacturers. This arrangement entailed certain risks over access to capacity and control of intellectual property that the availability of a "pure-play" foundry alleviated.

TSMC's chief rival is an older Taiwanese government-backed company, United Microelectronics (UMC), which sold off its design activities in the late 1990s and adopted the foundry model. The third biggest foundry, Chartered Semiconductor, is located in Singapore and is part-owned by the government.

The newest entrant, China-based Semiconductor Manufacturing International Corporation (SMIC), was founded in 2000 by Richard Chang, a Taiwanese expatriate with experience in Taiwan's foundry business following a U.S. graduate education and twenty years' experience at Texas Instruments. SMIC's investors include international venture capitalists and Chinese government entities. SMIC has successfully attracted a range of technology partners and customers, primarily from the United States, hired hundreds of Taiwanese engineers with foundry experience,[35] and listed its shares on the New York Stock Exchange in 2004.

The technology level of China's fabrication capability is theoretically limited by the Wassenaar Arrangement of 1996, by which more than thirty countries agreed to restrict exports of dual-use technologies that might undermine international security. Interpretation and enforcement, however, are left up to individual member states, and most countries with chip equipment industries other than the United States have been unwilling to curb exports of advanced chip-making equipment to China.[36] In 2003, the U.S. government issued SMIC a special license specifying that it does not make chips for military use, which allowed U.S. equipment makers to compete on a more even basis with their Japanese and European rivals.[37]

TABLE 2: Top Six Pure-Play* Foundries, 2004
(Total revenue $16,695 million)

Company	Country	2004 Revenue (US$ millions)	2004/2003 Growth	2004 Share of Total
TSMC	Taiwan	$7,648	31%	45.8%
UMC	Taiwan	$3,900	42%	23.4%
Chartered	Singapore	$1,103	52%	6.6%
SMIC	China	$ 975	166%	5.8%
Vanguard	Taiwan	$ 474	66%	2.8%
DongbuAnam	S.Korea	$435	32%	2.6%

Source: IC Insights, reported in "China gains in 2004 pure-play foundry rankings," EE Times, March 28, 2005.

* "Pure-play" foundries are those dedicated to foundry services and exclude companies that manufacture their own chips as well as offer foundry services.

The advent of government-funded manufacturing in Asia raised concerns about a potential loss of manufacturing jobs in the United States, especially since the U.S. semiconductor industry had seen its fortunes slip during the 1980s as U.S. DRAM makers lost market dominance to Japanese companies. However the Asian foundries contributed to the resurgence of the U.S. chip industry, since they facilitated the blossoming of design-only (or "fabless") chip companies, especially in California, during the 1990s.[38]

Over the last ten years, fabless revenue (C.A.G.R. of 20%) has been growing faster then the semiconductor industry as a whole (C.A.G.R. of 7%), and worldwide fabless revenue was

[35] "TSMC Sues SMIC," Electronic News, December 22, 2003.
[36] "Chip-equipment export rules to China are unclear and 'ineffective'," Semiconductor Business News, February 15, 2002.
[37] "SMIC obtains special license for advanced U.S. fab gear," Silicon Strategies, September 30, 2003.
[38] Macher, Mowery, and Hodges (1998).

$20.6 billion in 2003. Of the top thirty fabless firms that year, twenty were U.S.-based and had a combined revenue of $13.5 billion. The next most important location for fabless companies is Taiwan, where six of the top 30 firms (combined revenue of $2.8 billion) in 2003 were located.[39] Table 3 shows the top 10 fabless firms of 2004.

TABLE 3: Top 10 Fabless Companies, 2004
(Total Revenue: $33 billion)

Company (Location)	2004 Revenue (US $ millions)
Qualcomm (Calif.)	$3,224.0
Broadcom (Calif.)	$2,400.6
ATI Technologies (Canada)	$2,140.9
Nvidia (Calif.)	$2,010.0
SanDisk (Calif.)	$1,777.1
Xilinx (Calif.)	$1,588.7
MediaTek (Taiwan)	$1,252.5
Marvell Semiconductor (Calif.)	$1,224.6
Altera (Calif.)	$1,016.4
Conexant (Calif.)	$ 914.6

Source: Fabless Semiconductor Association, cited in "Worldwide Fabless Revenue Grew 27% in 2004, FSA Revealed," Nikkei Electronics Asia Online, March 18, 2005.

In addition to supporting the increasingly important fabless sector, the Asian foundries are also permitting integrated firms, from smaller players all the way up the world's third-largest chip firm, Texas Instruments, to hedge the enormous risk of building new factories by using the foundries for buffer capacity and even for fabricating leading-edge chips that have a short product life or uncertain volume.

The availability of buffer capacity in Asia has allowed chip producers to build less fabrication capacity, which reduces the risk of facing unutilized capacity with a large fixed depreciation expense. Fab-owning companies (called integrated device manufacturers, or IDMs) can keep their own fabs fully booked and shift excess demand to the foundries as needed. The foundries adjust their prices as their capacity utilization varies. IDMs began shifting business to foundries in the mid-1990s and in recent years have accounted for approximately 45% of foundry revenue.[40] Looked at another way, 20 to 25% of the value of the semiconductor industry is being manufactured on a (mostly-foreign) outsourced basis.[41]

Although the outsourcing trend represents a shift of manufacturing to Asia, it seems unlikely that the U.S. semiconductor industry will ever entirely cease domestic fabrication. At the leading edge, companies like Intel, IBM, and Texas Instruments derive advantage from implementing advanced process technologies for their flagship products at the earliest possible time. Companies like Freescale (formerly Motorola) and Micron benefit from running non-standard processes. In all these cases, fab ownership affords closer interaction between the design and manufacturing functions and helps to ensure the protection of key trade secrets. Nevertheless, as the foundries add capacity and smaller fab-owning firms decline to invest in new plants, the number of fab-owning firms will likely decline.

[39] Data from IC Insights reported in "SanDisk, Silicon Labs leap in 2003 fabless rankings," Silicon Strategies, March 18, 2004.
[40] Data reported by Semico Research Corp, reported in "System houses remain weak link for silicon foundries," Silicon Strategies, May 11, 2004.
[41] Authors' calculations, assuming that foundry revenue represents about one-third the value of the final chip price.

There is a limit to the eventual size of the foundry sector. For example, Intel will continue internal (but not entirely domestic) fabrication of its PC microprocessors because they depend on leading-edge process technology that is part of the company's competitive advantage.[42] Samsung, the leading memory maker, will continue internal fabrication of its memory chips, since they require high volume, low cost production runs with short product life cycles. Intel and Samsung, the top two semiconductor companies worldwide, accounted for 21.4% of industry sales in 2004.[43] The major category of chips that are manufactured by foundries are logic chips, including a range of general-purpose and application-specific products, and mixed-signal chips, which primarily use standard processes. All told, outsourced manufacturing, the bulk of which occurs overseas, will probably never exceed 50% of the semiconductor industry.[44]

B. Offshore fab investments

Another way to look at semiconductor fabrication in the United States is to consider where fab investment takes place, and the data reveal a growing shift away from U.S. investment in domestic fabs. These historical data come from our colleagues Leachman and Leachman (2004). Table 4 shows fab capacity in terms of where it's located in 1980, 1990, and 2001.[45] The shift of capacity from Japan and the United States to the rest of Asia (primarily South Korea and Taiwan) is striking. Japan and the United States accounted for 80% of fab capacity in 1980, but only 49% of capacity in 2001.

TABLE 4: Regional Location and Ownership of Worldwide Fabrication Capacity
(For each year, capacity location is shown on top and capacity ownership is shown beneath it in parentheses.)

Year	Asia ex-Japan	Europe/ Middle East	Japan	North America
1980	4% (3%)	16% (15%)	38% (37%)	42% (44%)
1990	12% (12%)	13% (9%)	45% (45%)	30% (36%)
2001	38% (39%)	13% (8%)	20% (24%)	29% (38%)

Source: Leachman and Leachman (2004), Tables 8.2, 8.4
Note: The ownership row total for 2001 adds to more than 100 because jointly owned capacity was credited in full to all owners.

However looking at the same data in terms of region of ownership (shown in parenthesis) show that, although the rise of capacity owned by companies in Asia ex-Japan mirrors the rise of location capacity, the decline of capacity owned by U.S. companies is less severe than the fall in capacity located in the U.S. Although only 29% of fab capacity in 2001 was in the United States, U.S. companies had ownership stakes in almost 40% of global capacity.

Because so many fabs owned by companies in one region are located in another, these data do not directly answer the question of how much U.S.-owned capacity is located outside the

[42] In addition to its multiple fabs in the United States, Intel fabricates microprocessors in Israel (since 1985) and Ireland (since 1993).
[43] Gartner Dataquest data reported in "Gartner differs with rivals in top-10 chip rankings," EE Times, March 23, 2005.
[44] See "More Changes Ahead for Foundries, Industry," Electronic News, December 4, 2003, for a similar analysis.
[45] Because older fabs use a range of wafer sizes and linewidths, the underlying data have been normalized using a capacity metric based on the number of functions, where a function is one memory bit or one logic gate.

United States. Rob Leachman generously helped us to make this calculation.[46] In 2001, approximately one-third of U.S.-owned capacity was located offshore as shown in Table 5. The offshore fabs were primarily in Japan and Europe, which reflects the rise of joint ventures to share risk as the cost of fabs increased. Conversely, about 22% of the fab capacity located in North America was owned by companies based in other regions (not shown).

TABLE 5: Distribution of North-American-Owned Fab Capacity, 2001

North America	65.4%
Europe/Middle East	18.6%
Japan	13.0%
Asia ex-Japan	3.0%

Source: Calculations courtesy of Rob Leachman.

The trend toward Asian manufacturing is continuing. The largest - and potentially most efficient - fabs today utilize 300mm (12-inch) diameter wafers.[47] Table 6 shows the geographical distribution of existing and announced capacity as of late 2004. Taiwan already has one of the largest concentrations of these mega-factories, which are needed by the foundries and memory chip producers to keep their unit costs low, even as it greatly increases their exposure to the risk of excess capacity. The major Japanese companies have also made a significant commitment to the technology, although most of these fabs are not yet in full operation. Leading U.S. firms, such as Texas Instruments, were early adopters of the 300mm technology, but are slowing down their commitment to new fabs, in part because of their ability to turn to foundries for buffer capacity. SMIC's newest fab constitutes China's entry in the 300mm list.

As of October 2004, thirty-six 300mm fabs were in various stages of construction in addition to the twenty-four already in production.[48] Each of these fabs requires annual revenues of well over $1 billion to be profitable.[49] As has occurred following previous construction cycles in the semiconductor industry, the new fabs will likely result in a period of overcapacity until demand grows sufficiently.

TABLE 6: 300mm Fabs Producing, Equipping, or Under Construction, Oct.2004

Japan	24%
U.S.	24%
Taiwan	19%
Europe	14%
S.Korea	12%
Singapore	3%
China	5%

Source: Strategic Marketing Associates (www.scfab.com), based on theoretical full capacity and on fab location. Total adds to more than 100% because of rounding.

[46] The Leachman data do not include ownership shares for jointly-owned fabs. We divided such fabs by the number of regions (2 or 3) involved in ownership to estimate the U.S. share. As much as 10% of U.S.-owned capacity was in joint venture fabs in 2001, but those fabs were spread across all regions, so our estimation error is not likely to be more than 1 or 2 % up or down from the figures in the table.

[47] Many of the 300mm generation of fabs are still being expanded to efficient scale. Projected cost savings of about 30% per chip are expected from these fabs when they are equipped to efficient scale and running at full capacity (Rob Leachman, personal communication, May 2005). When such fabs are not running at full volume, losses mount quickly because of the rapid equipment depreciation.

[48] Data from Strategic Marketing Associates (www.scfab.com).

[49] Authors' calculation, suggested by Toshihiko Osada, based on data in Appendix 2 of Howell and others (2003). Annual depreciation and operating expense for a U.S.-based 300mm fab running 6,000 wafers per week on a 90-nanometer process totaled $975,000.

C. Fabs and employment

This section discusses the impact of globalized fabrication on U.S. white-collar employment. Although the advent of outsourced manufacturing in Asia did not represent a transfer of capacity that entailed a shutdown of U.S. facilities, it has very probably reduced the number of facilities that would otherwise have been built here, which represents the loss of a number of potentially high-skilled jobs. TSMC, which accounts for about half the pure-play foundry market, currently operates one 300mm and five 200mm fabs in Taiwan (plus one in Washington state).

We have detailed staffing data on earlier-generation fabs gathered in the mid-90s by the Berkeley Competitive Semiconductor Manufacturing (CSM) Program.[50] The data describe the average employment distribution at a sample of fabs running 150mm and 200mm wafers in four countries.[51]

As wafer size increases, output rises for a given level of wafer throughput, and both materials handling and information systems become more automated to more safely handle the increased weight and value of each wafer and to minimize human error. Automation changes the composition of the workforce as the need increases for engineers and declines for operators. In the CSM data, engineers increase from 15% to 24% of the total workforce between 150mm- and 200mm-generation plants, with a corresponding decline in operators from 73% to 62% (see Table 7) even as the overall employment level of the fab stayed approximately the same at about 750 workers.

TABLE 7: Work Force Composition
(Mean Headcount in Matched 150mm and 200mm Fabs)

	150mm	200mm
Operators	547 (73%)	470 (62%)
Technicians	91 (12%)	107 (14%)
Engineers	114 (15%)	181 (24%)
Total	752	758

Source: Brown and Campbell, 2001.

The shifting of jobs from operators to engineers in the transition from 150mm to 200mm fabs results in the growth of engineering jobs paying from $29,000 to $56,000 per year and the decline in operator jobs paying $14,000 to $37,000 per year (see Table 8). The initial pay of technicians and engineers is over one-third higher in the high-tech 200mm fabs, and their pay premium compared to operators has increased.

[50] The CSM program is a multi-disciplinary study of the semiconductor industry established in 1991 by a grant from the Alfred P. Sloan Foundation with additional support from the semiconductor industry. Further details are available at esrc.berkeley.edu/csm/.

[51] Twenty-three fabs in four countries were part of the CSM survey. For this table, the 150mm wafers fabs were matched to the 200mm wafers fabs by company, so that the company human resource policies are comparable between the two groups, which reduced the sample to fourteen.

TABLE 8: Work Force Compensation
(Mean Wage or Salary in Matched 150mm and 200mm Fabs)

	150mm		200mm	
	Initial pay	Maximum pay	Initial pay	Maximum pay
Operators (hourly)	$5.88	$15.47	$7.12	$18.44
Technicians (hourly)	$6.68	$11.50	$9.12	$15.83
Engineers (monthly)	$1,785	$5,019	$2,381	$4,689

Source: Brown and Campbell, 2001.

A look at the returns to experience, which are proxied by the maximum pay, shows that engineers fare less well. Experienced technicians and operators have the same pay improvement in the 200mm fab as do the new hires. However, the experienced engineers are losing out over time as their mean maximum salary is actually lower in the 200mm fabs. In interviews, we learned that fabs liked having young engineers with knowledge of new technology, and they did not worry about losing older engineers. Over time, consequently, fabs were willing to increase wages of new hires without raising the wages of experienced engineers. Rapidly changing technology plus an ample supply of new hires and low turnover allowed the companies to flatten engineers' career ladders with no adverse consequences.

We do not have comparable data for the 300mm fab, which typically costs $2-3 billion (depending upon the size), has 100% automation of materials handling and wafer processing, and fabricates a wafer that is 2.25 times larger than the 200mm wafer. The overall cost per chip in the 300mm fab is more than 30 percent lower compared to the 200mm fab.

Because these new 300mm fabs are processing advanced circuits, such as those using 90nm processes, the amount of inspection, metrology steps, and in-line engineering-related activities are significantly higher than their older 200mm counterparts for the same wafer throughput. As a result, most of the 300mm worker savings achieved with the automation of materials handling, often cited to allow approximately 30% less labor input, is now being re-applied to the new engineering tasks, which are much higher value added and more intellectually challenging, and include more troubleshooting. Therefore the number of workers has not been reduced as a result of the advanced factory automation; instead there has been a shift in task composition. The percentage of workers with higher engineering and technical problem-solving skills has greatly increased, while the percentage of workers needed for wafer movement and equipment starting and stopping has greatly decreased. However the proportion of engineers has not increased.[52]

So what is the net employment impact of fabrication offshoring? According to the Semiconductor Industry Association, U.S. chip firms employed 103,000 engineers in 2003, of which 30% were located offshore. The share of offshore employment had not grown since 1998, and in fact fell during the Internet/telecom bubble before returning to 30%.[53]

As a back of the envelope calculation, we estimate that if all foundry production were based in the United States instead of Asia, it might add 11,000 jobs, of which some 2,600 would

[52] Personal communication, April 2005.

[53] Data are from the annual SIA Semiconductor Workforce Strategy Committee Survey, referenced in "SIA Workforce Strategy Overview," a presentation by David R. Ferrell to the Electrical and Computer Engineering Department Heads Association annual meeting, March 22, 2005. Accessible as of April 21, 2005 at www.ecedha.org/Temp04-05/agenda.html.

be highly-paid engineers.[54] But it must be noted that not all foundry sales are to U.S. customers. In 2003, for example, half of TSMC's gross revenue came from non-U.S. sources.[55]

As a point of comparison, the Fabless Semiconductor Association reported that publicly-traded fabless companies in North America employ approximately 45,000 workers as of December 2004.[56] A review of company information suggests that more than half of these are software or hardware engineers, although an unknown share of them are located offshore.

To summarize this section, offshore investments in fabrication were driven by market access concerns more than by cost reduction, and have been at least partially offset by reciprocal investments from leading foreign producers. Meanwhile, the availability of outsourced fabrication in Asia played to the U.S. strength in design by facilitating the emergence of the fabless chip industry. The Asian foundries are probably also part of a long-run reduction of U.S. chip manufacturing, but any loss of U.S. manufacturing jobs has been gradual, and the loss of chip manufacturing jobs to foundries has probably been offset to some extent by the increase in design jobs. The reliance of the U.S. semiconductor industry on high-end design jobs is one of the reasons that chip design, the latest frontier for offshoring, which is addressed in the next section, may be a cause for greater concern.

IV. Offshore Design

The picture for offshore design by U.S. semiconductor companies is still taking shape. Although some design has been done offshore since at least the 1970s, the pace of offshoring has noticeably increased in the last few years, and there is growing evidence that the U.S. market for chip design engineers has been adversely affected.

A. The economics of chip design

Chip design is highly skill-intensive, since it employs only college-trained engineers. A couple of medium-size chip designs will employ as many electrical engineers as a fab for a year or more (although the skills are not directly transferable). A complex chip design like Intel's Pentium 4, with 42 million transistors on a 180nm linewidth process, engaged hundreds of engineers for the full length of the five-year project.[57] Design teams can also be as small as a few engineers, and project duration varies from months to years. Team size depends on the complexity of the project, the speed with which it must be completed, and the resources available.

The design of an integrated circuit is a hierarchical procedure that passes through identifiable stages with feedback as needed. With considerable simplification, the stages are specification, logic design, and physical design. Once the chip has reached the prototype stage, it needs to be validated in a hardware simulation of a complete system. Parallel with this process, the design must be repeatedly verified, and the software that will be part of the chip, and that will run on it, needs to be written.

The highest-level design stage is the general specification for how the chip as a whole will behave within the system of which it's a part. This is a high-value-added function that applies the company's market knowledge and intellectual property in deciding what feature set will be most profitable.

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[54] TSMC, which accounts for about half the foundry industry, has one 150mm, one 300mm, and five-and-a-half 200mm fabs outside the United States. These fabs probably have different rated capacities, but we can approximate employment by calculating 750 workers per plant, which works out to 5,625. Doubling that to approximate the entire foundry sector brings us to 11,250.

[55] Note 27c of Form 20-F filed by TSMC with the Securities and Exchange Commission for fiscal year ended December 31, 2003.

[56] FSA "Global Fabless Fundings and Financials Report, Q4 2004".

[57] "Comms held Pentium 4 team together," EE Times, November 1, 2000. "Linewidth" refers to the size of the features etched on a wafer during the fabrication process. Each semiconductor process generation is named for the smallest feature that can be produced.

The next stage, logic design, uses symbolic abstractions to describe how signals will be processed within the chip, first at the register level, then at the gate level.

The final stage, physical design, involves the translation of the abstract version into a map of actual wires and devices interconnecting across multiple layers on the silicon surface.

Electronic design automation (EDA) includes both the use of software tools by engineers to realize their designs and the actual automation of specific parts of the design with less engineering input, especially at the later stages of mainstream digital designs.

Table 9 shows the change in the effort required at each stage of design over succeeding generations of process technology, from 350 nanometer linewidths, first introduced in the mid-1990s, to 130nm, which entered volume production in 2003. The underlying project is assumed to be a digital logic design, the industry's typical product. Other types of design, such as analog or memory chips, require different engineering inputs. The overall chip is assumed to be more complex at each linewidth as miniaturization allows more functions to be packed onto a chip. In raw terms (transistors per engineer per year), design engineer productivity improved by a factor of more than 20 during the 1990s.[58]

TABLE 9: Engineer Hours to Design 1 Million Logic Transistors

	350nm	250nm	180nm	130nm	Change from 350nm to 130nm
Specification	23.0	29.8	91.4	271.6	1081%
Logic Design	714.2	738.4	756.4	837.7	17%
Physical Design	311.0	357.2	391.7	473.5	52%
Validation	103.7	127.6	164.5	197.4	90%
Software	378.4	672.4	985.7	1798.3	375%
Total	**1530.3**	**1925.4**	**2389.7**	**3578.5**	**134%**

Source: International Business Strategies (2002), used with permission.

Note: The average number of transistors in a typical logic design increases by a factor of about two with each reduction in linewidth. The table normalizes the hours required for 1 million transistors at each generation based on the assumption that the underlying project is increasingly complex: 2 million transistors at 350nm, 5 million at 250nm, 20 million at 180nm, and 40 million at 130nm.

The biggest changes involve the importance of software in the design process, which now accounts for one-half of the total engineer hours. Although software is typically not considered part of chip design as such, software expertise is increasingly important for the competitive advantage of semiconductor firms.[59] Chips today are often integrated to system-level complexity because of the size, reliability, and other advantages this brings. Greater integration means that the system software must be generated in parallel with the system-level chip for reasons of coherence and, especially, time-to-market. It is this need to plan carefully for the hardware-software co-design that has caused the specification portion of chip designs to explode by 1081% over the last four technology generations.

The software effort itself has increased by 375%. According to one software executive, a typical chip in 1995 went into a stand-alone product and required 100,000 lines of code. In 2002, a typical chip for a networked programmable product requires a million lines of code.[60]

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[58] Semiconductor Industry Association (2003).

[59] Linden, Brown, and Appleyard (2004).

[60] Jerry Fiddler, chairman of Wind River Systems, cited in "Keynoter says chip value is in its intellectual property," EE Times, June 14, 2002.

The software, plus the greater complexity of chips themselves, has caused design validation hours to grow by 90% for each million transistors.

By comparison, the growth levels for the actual design engineering jobs of logic and physical design for each million transistors are a relatively modest 17 and 52%, respectively. This is largely because, as chips have gotten more complex, the process of chip design has become more automated.[61] The number of transistors that can be fabricated on a given area of silicon has doubled every 18 months for roughly 40 years, a phenomenon known as "Moore's Law," after Gordon Moore, one of the founders of Intel. In the early 1960s, digital ICs contained fewer than 50 transistors.[62] The industry can now place some 100 million transistors on a chip, and Intel predicts a billion-transistor processor by 2007.[63]

The automation that enables the design of today's complex chips has evolved in parallel with the rise in complexity. At the beginning of the industry, designs were hand-drawn and hand-transferred to a template that was used to make the actual circuit. In the 1970s, the later stages of the process were computerized, and in the 1980s they were automated.

The introduction of automation, along with the advent of high-bandwidth telecommunications, gave chip companies the ability to subdivide the design process across multiple locations.

These advances pertain primarily to digital designs, i.e., those that work on binary streams of data. Designs that utilize all, or mostly, analog circuits, which process continuous signals such as sound waves, are also done with EDA tools, but are not so easily automated and require more experienced designers with specific training.

We now consider, in turn, the in-house offshoring and international outsourcing of chip design.

B. Offshore design

The in-house offshoring of chip design can occur for any of the three reasons pertaining to competitive advantage: closer contact with customers, access to specialized skilled labor, and cost reduction.

Most early offshore design investments by U.S. companies through the 1970s, like offshore fabrication investments of the same period, were market-driven and limited to Japan and Western Europe.[64] By the mid-1980s, a handful of offshore design investments had been made in Hong Kong, Taiwan, Singapore, which are the more advanced economies of East Asia outside Japan.[65] These design centers were dedicated to adapting existing chips to local market needs.[66]

The prime example of the market access motivation for offshore investment is the "application-specific" IC (ASIC), a logic chip designed for a specific customer. U.S.-based ASIC producers like IBM and LSI Logic have established design centers in all major markets of Europe and Asia to facilitate the interaction of their engineers with their customers. These companies also maintain other offshore design centers that develop the "cells" or building blocks that are later combined in various ways, and these centers may be low-cost seeking or skill-seeking.

Specialized skills are an important reason that U.S. semiconductor companies invest overseas. Britain, for example, has developed expertise in consumer multimedia, and Scandinavian countries are noted for their skills in wireless network technology. These specialized skill bases are often accessed by acquisition of an existing company that continues as a subsidiary. Examples abound. In 2000, Broadcom acquired Element 14, a British fabless company with 68 employees specializing in central office ADSL technology that became

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[61] Hemani (2004).
[62] Borrus (1988, p. 75).
[63] "Intel readies road map for billion-transistor processors," EE Times, January 4, 2002.
[64] Henderson (1989 p. 48).
[65] ibid. (Figure 4.2).
[66] ibid. (p. 58).

Broadcom UK Ltd.[67] In 2001, Agilent acquired Sirius, a Belgian designer of cellular chips for the CDMA standard with 19 employees, and made it a research and design center for next-generation cellular technology.[68] In 2005, Intel acquired Oplus, a successful maker of chips for digital television with 100 workers and that will remain an independent subsidiary.[69]

As was true of fabrication, in-house design offshoring works both ways, and many foreign companies maintain a Silicon Valley or other U.S. design center to take advantage of the high skills and productivity available there as well as have access to U.S. customers. Philips of the Netherlands, for example, bought VLSI Technology, a major ASIC company with over 2,000 employees (about one-third of whom were fab workers), in 1999 for nearly $1 billion.[70] Hitachi Semiconductor has a U.S. design group several hundred strong.[71] Toshiba has a network of seven ASIC design centers around the United States.[72] Even foreign start-ups may need to have a U.S. design team to work with U.S. customers or to access leading-edge analog design skills.

The category of in-house design offshoring that is perhaps growing the fastest – or at least getting the most attention – is cost reduction. For Silicon Valley firms, some cost reduction is available by opening satellite design centers elsewhere in the U.S., where some locations have average engineering salaries that are up to 20% lower than salaries in the Silicon Valley. But these salaries are still much higher than salaries in India and elsewhere, as discussed below.[73] The prospects for cost reduction offshore are better than ever because of changes in the last 20 years that have seen high-bandwidth infrastructure extended around the globe and the economic liberalization of large economic areas in Eastern Europe, and especially Asia.[74]

Dividing chip designs across locations presents a number of managerial challenges, as we have learned from interviews and press reports. The sacrifice of face-to-face interaction between different parts of the design team can adversely affect productivity, and distance makes it harder to evaluate and reward individual contributions to team performance. Task assignments must be more carefully codified for offshore teams than for locally-based engineers, and managers will need to travel periodically between locations. When the separation is across borders, there are also cultural differences that can make communication less effective. An Intel engineer was reported to say that cultural differences were the single biggest problem in managing design teams between California and Israel, and this separation did not include any language differences.[75]

Cost-driven in-house offshoring incurs other costs that partially offset the difference in salaries, especially during the early stages of establishing an offshore design center. One that is often mentioned is the lower quality and productivity of inexperienced engineers. This raises monitoring costs, and offshore engineers may also require a longer training period than a U.S. team would need. Additional controls may also be needed to protect key intellectual property. According to a venture capitalist, the actual savings from going offshore is more likely to be 25 to 50% rather than the 80 to 90% suggested by a simple salary comparison.[76]

Design offshoring can run up against national security barriers. For example, the U.S. government has placed limits on the export of advanced encryption technology. Communications chips that employ such technology are difficult to design offshore. Either the chip design must be

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[67] "Broadcom acquires Element 14 for $600 million, enters ADSL chip market," Semiconductor Business News, October 4, 2000.
[68] "Agilent to buy Belgium's Sirius to offer new CDMA chip solutions," Semiconductor Business News, May 21, 2001.
[69] "Intel buys into consumer sector with Oplus acquisition," Silicon Strategies, February 24, 2005.
[70] "Philips to acquire VLSI Technology for $953 million," Semiconductor Business News, May 3, 1999.
[71] "Hitachi Forms North America Semiconductor Systems Solutions Unit," Hitachi Press Release, September 2, 1998.
[72] "Toshiba Expands Soc Design Support Network With Opening Of San Diego Design Center," Toshiba Press Release, November 26, 2002.
[73] "Mean wages edge closer to six-figure mark," EE Times, August 25, 2004.
[74] Ernst (2004).
[75] "Global chip design raises promises and challenges," EE Times, January 11, 1999.
[76] Interview, May 2004.

compartmentalized, with the encryption block designed only in the United States, or government approval, subject to possible delays, must be obtained in advance.[77]

Yet despite these pitfalls, the amount of offshore design in industrializing economies has noticeably expanded over the last decade. Some companies value the opportunity to design on a 24-hour cycle because of the enormous pressure to reach the market ahead of, or no later than, competitors. One established U.S. chip company adopted a rolling cycle between design centers in the United States, Europe, and India.[78] More common is the bi-national arrangement used by a Silicon Valley start-up that had all of its design beyond the initial specification done by a China subsidiary established only months after the head office was set up. Ten executives in the head office had to train the mostly inexperienced staff in Beijing, which was about thirty strong.[79] The Silicon Valley staff would review Beijing's work from the previous day then spend up to three hours on the phone (starting around 5pm California time) providing feedback and reviewing assignments for that day in Beijing. In a single-location firm, this work-feedback cycle would take two days.

Venture capitalists have reportedly begun to require start-ups to include some offshoring in their business plans in order to better leverage their resources. A typical comment is, "We don't fund chip designs that don't outsource to India. If you rely on Indian contractors for the things they do well, you can get a chip out for under $10 million. If you don't, you can't, and you won't be competitive. It's that simple."[80] PortalPlayer, the company behind the key multimedia chip in Apple's iPod, is a recent example of a successful start-up that set up an Indian software and chip design subsidiary within a few months of its founding in 1999.[81]

We will discuss offshore subsidiaries again below.

C. Domestic and foreign outsourcing of design

Low-cost design engineering resources can also be tapped through international outsourcing, although to date most design outsourcing by U.S. companies takes place domestically. All parts of a design, including the whole procedure from specification to finished chips, can be outsourced. In addition to the traditional work-to-order model, companies can also license standardized functional sections (e.g., a USB interface) of a system-level chip designed at the logic or physical level to save time. These reusable modules are known in the industry as "cores" or "IP blocks".[82]

The easiest part of chip design to outsource is physical design because it is a relatively standardized task. It is also the least sensitive part of design in terms of revealing the customer's intellectual property. However for designs requiring leading-edge process technology such as 90nm linewidths, layout has become much less straightforward because of the sensitivity of the atomic-scale wiring. In such a case, physical design is likely to be outsourced only by small and medium companies that lack the resources to develop the necessary expertise in-house. On the other hand, we interviewed one (well-funded) start-up whose initial design was so complex that outsourcing any parts wasn't an option.[83]

Another design functions that is frequently outsourced is logic verification, the resource-intensive task of making sure that that first stages of the physical implementation are a correct translation of the abstract logic. At the other extreme, architectural design, or the design of key

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[77] Interview, December 2004.
[78] Interview, April 1998.
[79] Interview, August 2004.
[80] William Quigley, managing director at Clearstone Venture Partners (Menlo Park, Calif.), quoted in "Venture capitalist explains new rules for IC startups," EE Times, January 16. 2003.
[81] "Designs for Digital Audio, Auto Electronics," Nikkei Electronics Asia, October 2002.
[82] Linden and Somaya (2003).
[83] Interview, November 2004.

functional blocks containing proprietary algorithms are the least likely to be outsourced because of the risk of exposing proprietary knowledge.[84]

The availability of outsourcing (foreign or domestic) is particularly important for small companies and start-ups because of the relatively large fixed cost of EDA tools, which are typically licensed per engineer. One consultant estimated that the minimum annual software expense for a small company is $10 million.[85] For the industry as a whole, EDA expense runs close to 1% of revenue. In that case, a company earning less than $1 billion in revenue would be below the efficient scale for in-house design. Only the nine largest fabless companies met that criterion in 2004. One consultant estimated that outsourcing even within the United States would save a small start-up that does fewer than five designs a year up to two-thirds the cost of doing the work in-house.[86]

Another type of customer for outsourced design services are the systems companies, such as Apple Computer or Cisco. Although these companies often design chips in-house either to protect intellectual property or to reduce the cost of custom chips, they may turn to outside (and possibly offshore) service providers for part of the design process.

A great deal of outsourcing takes place in the United States. Many interviewees reported that they outsource physical design to small local companies on an as-needed basis. The leading suppliers of design services worldwide are the leading design automation software vendors, Cadence Design Systems, Synopsys, and Mentor Graphics. Their annual services revenue is about $300 million out of a total outsourced design market estimated at $2.5 billion.[87] As this suggests, the remaining market is highly fragmented.

As might be expected from the increasing interaction of physical design with advanced processes mentioned previously, foundries work closely with design services providers. TSMC and UMC each have equity ties to a Taiwanese design service provider (Global UniChip and Faraday, respectively). In China, the emergence of low-cost foundries have also given rise to design services companies. The most advanced of these, IPCore and VeriSilicon, were both founded in 2001 by executives with years of experience in U.S. and Asia. In India, despite the lack of any significant chip manufacturing, large IT service providers such as Wipro and Tata Consultancy Services have expanded into semiconductor design services for international clients. Elsewhere, there are dozens of companies around the world able to help customers complete all or part of their chip designs. However most of the concern about foreign competition from low-cost chip designers focuses on China, Taiwan, and India, which are the countries that we believe will have the greatest impact on the availability of design engineers outside the United States in the years ahead.

D. Chip design in Asia

Offshore design is driven in part by the steady advance of semiconductor process technology, which has created vast areas of "silicon real estate" for complex chips that could potentially be designed. The inability of design automation to keep pace with Moore's Law is sometimes referred to as a design "productivity gap."[88] The gap is to some extent exaggerated, since a relatively small percentage of designs are done at the leading edge in any one year.[89] Nevertheless, there is an acknowledged need for more design engineers than are available in the

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[84] "Outsourcing trend proves: Complex by design," EE Times, January 31, 2005, and interview, April 2004.
[85] International Business Strategies (2002).
[86] Interview, April 2004.
[87] "Complex chips reignite demand for design services," EE Times, October 11, 2004.
[88] Semiconductor Industry Association (2003).
[89] "SOC-Mobinet, R&D and Education in SoC Design," presentation by Hannu Tenhunen at International Symposium on System-on-Chip 2004, Tampere, Finland on November 16-18, 2004, accessible at www.cs.tut.fi/soc/Tenhunen04.pdf as of April 19, 2005.

United States, especially those with systems and analog skills, as the industry continues to grow amid the increase in design complexity.

For a clearer picture of the global market for design engineers, Table 10 provides rough estimates for chip designer salaries, the number of annual engineering (excluding software) college graduates, the number of active chip designers (excluding embedded software), and a rating of the intellectual property protection regime in the United States and the four key Asian countries. The numbers, which are based on a combination of published sources and interviews, suggest that engineers in the United States and Japan earn much higher pay compared to Asian engineers.

These data are imprecise and intended as a general guide only. The salaries are rough estimates, and their variance is large. The salaries are for engineers with five or more years experience in the U.S. and for engineers aged 40 in Japan, since that is the approximate age they exit the union and begin to experience greater salary increases. The design engineers in the other countries tend to be younger and less experienced, but wages are reportedly rising rapidly in China and India. For example, the salary range offered for a design engineer with one to three years experience by SanDisk in Bangalore at jobstreet.com in June 2005 was $9,200 to $18,400 (at 43.52 Indian Rupees to the dollar).

TABLE 10: Recent Engineering Statistics, Selected Countries

	Annual design engineer base salary	Annual engineering bachelor degrees conferred (1997, except as noted)	Number of chip designers	Intellectual property protection, 2002 (10=high)
United States	$ 82,000	60,000	45,000	8.7
Japan	$ 60,000	100,000	--[a]	6.2
Taiwan	$ 30,000	13,000	14,000	6.7
China	$ 15,000	150,000	7,000	4.0
India	$ 15,000	30,000 (1990)	4,000	4.2

[a] We have been unable to obtain an estimate for the number of chip designers in Japan.
Sources: U.S. salary from 2004 BLS Occupational Employment Statistics web site (average for electronics and software engineers in NAICS 334400, Semiconductor Industry); Japan salary (average for circuit designer and embedded software engineers aged 40 years old) from Intelligence Corporation's data on job offers in 2003; Taiwan salary information from March 2005 interview with U.S. executive in Taiwan; China and India salaries are estimated based on a combination of interviews, business literature and online job offerings; number of degrees from Appendix Table 4-18, "Science and Engineering Indicators 2000," National Science Foundation; number of chip designers in U.S., China, and India from iSuppli as reported in "Another Lure Of Outsourcing: Job Expertise," WSJ.com, April 12, 2004; number of chip designers in Taiwan from interview with Taiwan government consultant to industry, March 2005; Intellectual property protection data from World Economic Forum as cited in Economic Freedom of the World, 2004 Annual Report, Chapter 3 (Vancouver, Canada: Fraser Institute). All numbers rounded to reflect lack of precision.

The salary gap is narrower for comparable key employees. One report claimed in 1999 that the salary ratio between the U.S. and India for experienced design engineers or managers was only 3-to-1.[90] Profit sharing bonuses vary over the business cycle in the U.S. and Taiwan, and can

[90] "Special report: India awakens as potential chip-design giant," EE Times, January 22, 1999.

be an important part of compensation. Benefits, which include health insurance and Social Security,, and options also cloud the picture in the U.S.

The other columns of Table 10 also must be interpreted carefully. The number of engineering graduates is only an indicator of political and social commitment to the discipline and does not translate to chip design capability. According to some sources, the number of chip designers being added each year in India and China is on the order of 400 each.[91]

Even the stated number of chip designers in the third column can be misleading, since there is confusion about the definition of "chip designer". One industry executive claimed that the number of "qualified IC designers" in China is only 500.[92] A Taiwan consultant didn't even consider the later (and lower-skilled) stage of physical design, called "place and route," to be part of chip design.[93] This group amounts to about 30% of Taiwan designers as we count them in the table.

Lastly, weakness in the ratings on intellectual property protection may be driven by lapses in specific sectors such as pharmaceuticals, trademark goods, or recorded media, that are not relevant to the semiconductor industry.

Despite their lack of precision, these data indicate that Asian design engineers, especially from the emerging giant economies of China and India, represent an important source of supplemental engineering talent as well as a possible competitive threat.

To attempt to get a clearer picture of the world-wide availability of "qualified IC designers," we consulted the Institute of Electrical and Electronics Engineers (IEEE), the leading professional organization for engineers, with almost 40% of its 365,000 members located outside the United States.[94] Of IEEE's several technical societies, the one most closely associated with chip design is the Solid-State Circuits Society (SSCS). Among other benefits, membership in the SSCS reflects an interest in accessing the latest research in the field.[95] We looked at the geographic distribution of membership in 2001, and compared it to 1991 (estimated) for individual countries.[96] We limited our attention to a mix of developing and developed countries with an active commercial chip-design sector (see Figure 1).[97] Because the U.S. dominates membership and requires a different scale, it is not shown in Figure 1.

In 2001, the SSCS had 19,715 members worldwide, of whom 56% were outside the United States. This was up from 13,788 in 1991, when only 45% were outside the United States. Among the countries shown, China, Taiwan and India had three of the four fastest growing SSCS memberships. The United States had 8,747 SSCS members in 2001, which is estimated to have grown 16% over the preceding decade, which is less than the growth rate for all countries shown except Canada (14%).

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[91] For India: "Designs on the future," IT People, February 10, 2003; for China: "China's Impact on the Semiconductor Industry," PriceWaterhouseCoopers, December 2004, p.7.

[92] "China's Impact on the Semiconductor Industry," PriceWaterhouseCoopers, December 2004, p.7.

[93] E-mail exchange, March 2005.

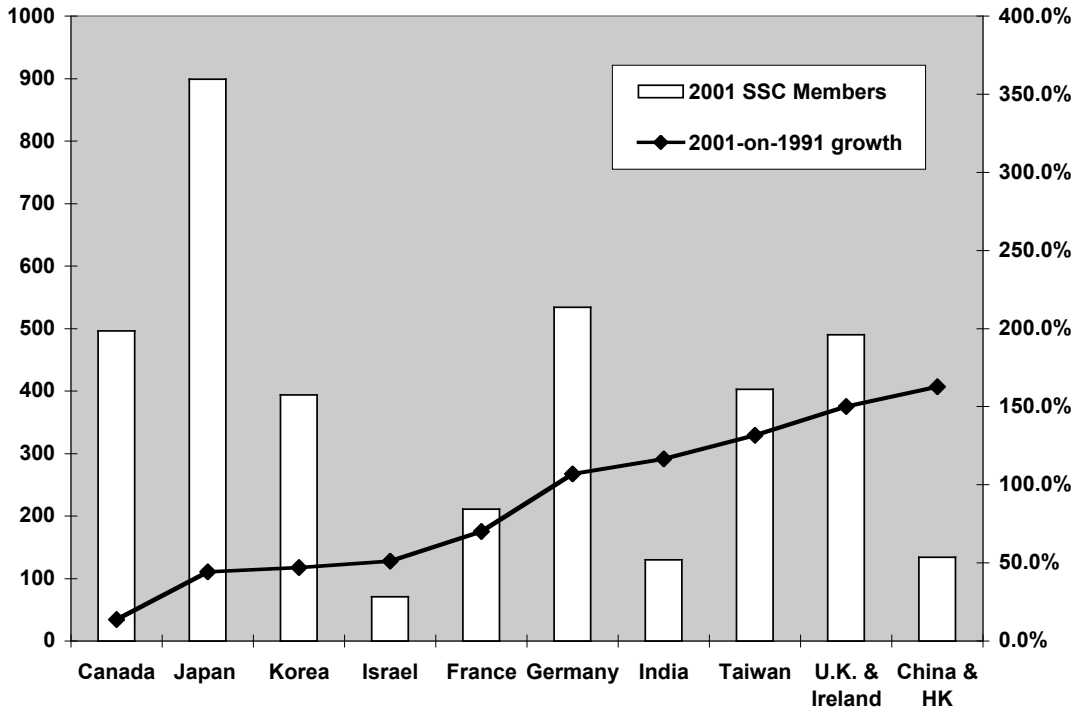
[94] From "IEEE Quick Facts," current as of January 2005. Accessed in April 2005 at www.ieee.org/portal/site/mainsite/menuitem.818c0c39e85ef176fb2275875bac26c8/index.jsp?&pName=corp_level1&path=about/&file=quick_facts.xml&xsl=generic.xsl

[95] This has become less true in recent years now that libraries at universities and elsewhere offer electronic access to IEEE publications. The data presented here end in 2001 when this was less an issue.

[96] Solid-State Circuits was a "Council" prior to 1997, when it became a society. Our colleague David Hodges, a member of the SSCS Administrative Council, suggested a means of estimating the 1991 membership by using a ratio involving two of the old council's sponsoring societies. Details available on request.

[97] The top three countries for growth during the period were Poland, Malaysia, and China, but the first two grew from very small bases (only four and five members, respectively, in 1991).

FIGURE 1: Solid State Circuits Society Membership (2001) and Growth (1991-2001), selected countries outside the U.S.



Source: IEEE data and authors' calculations.

How do these three countries compare in their chip design capabilities?

Taiwan has the most well-established chip design sector of the three, having benefited from focused government programs and the return of U.S. educated and trained engineers during the late 1980s.[98] The Taiwanese chip design sector is mostly locally-owned, with a few multinational companies also operating design subsidiaries. Taiwanese companies have particularly embraced the fabless model, with some 60 fabless companies listed on the Taiwan Stock Exchange in December 2004.[99] By comparison, there were about 70 fabless companies listed on NASDAQ at that time. The 2004 output value of all Taiwan's locally-owned design companies (including fabless and design service companies) was reported by the Taiwan Semiconductor Industry Association to be $8.15 billion.[100] One advantage for these firms was the availability of an important local market since many Taiwanese companies design, assemble, and procure components for computers, communication equipment, and consumer electronics for world-famous brands including Hewlett-Packard, Nokia, and Sony. In 1999, 62% of Taiwan's chip design revenue came from local sales.[101]

While Taiwan's design teams were praised in our interviews for their execution, which is a vital trait in an industry where time-to-market is often the difference between profit and loss, Taiwanese companies were mostly fast followers. Ironically, they are locked in to some extent by their reliance on business from the local systems firms, who are themselves as much as a

[98] Saxenian (2002).
[99] FSA "Global Fabless Fundings and Financials Report, Q4 2004".
[100] NT$260.8 billion converted at NT$32:US$1. Datum from "TSIA: Taiwan's 2005 semiconductor production value to rise 6.7% on year," DigiTimes.com, March 18, 2005.
[101] data from Taiwan's Industrial Technology Research Institute cited in Table 5, Chang and Tsai (2002).

generation behind the leading-edge technology.[102] From a U.S. perspective, Taiwanese competition for chips using last-generation technology has shortened the market windows during which U.S. chip companies can recoup their investments.

Taiwan's government has instituted several programs to improve the local design sector, including a plan to train several thousand new design engineers in Taiwan's universities, the creation of an exchange where local chip design houses can license reusable functional blocks, and an incubator where early-stage start-ups can share infrastructure and services.[103] Another initiative aims to attract chip design subsidiaries of major semiconductor companies, with early takers including Sony and Broadcom (a major U.S. fabless company). In 2000, a government research institute created the SoC Technology Center (STC) to design functional blocks that can be licensed to local companies, a model Taiwan has used successfully in other segments of the electronics industry. The STC has over 200 engineers, most of whom have a Master's degree or better[104]

China appears to be following a similar pattern to Taiwan: government sponsorship, local access to system firms such as Haier, Huawei, and TCL that are increasingly engaged in world markets, and active involvement of expatriates returning from the United States.[105] As of 2003, China claimed to have over 400 fabless design firms with total revenue of $547 million.[106] Many of these are small, poorly managed and rapidly running through their seed money before they can bring a product to market.[107] One interviewee, echoed by others, claimed that many, if not most, firms outside the top 10 - whose total revenue was $328 million in 2003 - are engaged in various types of reverse engineering, much of which is illegal.[108] Foreign firms are often reluctant to bring lawsuits for fear of displeasing the authorities and the unlikelihood of winning in Chinese courts, but at least two U.S. companies are suing Chinese rivals in export markets for intellectual property violations.[109]

China is not yet an important destination for design offshoring. Of the fifteen top U.S. semiconductor companies, a handful have opened research centers in China (compared to thirteen in India) as of June 2005, but most of these are targeting the local market for the time being, and, according to press reports, some are engaged in software or system design rather than chip design *per se*. Concerns over intellectual property protection appear to pose a greater barrier to foreign design activity than in India.[110]

Chip design in China is at an early stage. Its relatively young chip design engineers will steadily build their experience. Some companies, particularly those whose founders include expatriates returning with foreign experience, will likely begin to impact global markets by the end of the decade. It is too early to predict the eventual relative importance of domestically-owned and foreign-owned chip design activity, and whether domestic firms will be involved mostly with contract services or with creating and selling their own chips.

The Chinese government has taken many steps in support of chip design firms, some of the largest of whom are state-owned. Measures include tax reductions, venture investing,

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[102] Breznitz (2005).
[103] "Trends in SOC design unthaw at SOC 2004," EDN, December 9, 2004.
[104] SoC Technology Center interview, March 2005. "SoC" is a common industry acronym for "system-on-a-chip" meaning a complex semiconductor. integrating multiple functions.
[105] Saxenian (2002).
[106] Chinese government data cited in "TSMC: China IC design industry only a few years behind Taiwan," DigiTimes.com, September 10, 2004.
[107] Assessment of Byron Wu, iSuppli analyst, reported in "Analyst: China's IC design houses struggling for survival," EE Times, May 20, 2004.
[108] Interview with a European chip executive, conducted by Elena Obukhova in Shanghai, December 2003.
[109] See "An offshore test of IP rights," Electronic Business, May 2004; and "SigmaTel Sues Chinese Chipmaker over IP," Electronic News, January 6, 2005.
[110] "SIA Pushes Steps to Better IP Protection in China," Electronic News, November 17, 2004.

incubators in seven major cities, and special government projects.[111] A value-added tax preference for domestically-designed chips was phased out under U.S. pressure, and will reportedly be replaced by a WTO-friendly R&D fund.[112]

India presents a very different picture, with benign neglect by the government, a lack of manufacturing for chips and systems, and weaker levels of brain circulation with its U.S.-based expatriates.[113] Unlike Taiwan and China, India has no high-volume chip manufacturing, although construction has reportedly begun on a 200mm fab near Hyderabad with backing by a non-semiconductor firm from Korea and the Andhra Pradesh state government.[114] Perhaps because of India's weakness in chip and electronics manufacturing India has no major fabless companies (i.e. companies designing chips for sale under their own brand), and its chip designers provide design services or work at the subsidiaries of foreign chip companies, especially U.S. and European firms. Design services revenues for Indian companies in 2001 were $149 million.[115] The government is in the early stages of developing policies to support domestic chip design firms.[116] It is in the foreign subsidiaries that most of India's chip design is taking place.

The foreign chip companies were attracted by Indian engineers' use of English and the successful Indian software sector. Many of the early Indian investments by chip companies were software-focused, writing the microcode that becomes part of the chip. Over time, the Indian affiliates have taken on a bigger role, eventually extending to complete chip designs from specification to physical layout. This transition can happen quite quickly. Intel, for example, opened a software center in Bangalore in 1999, then started building a design team for 32-bit microprocessors in 2002.[117]

A number of U.S. semiconductor companies have software and chip development operations in India, including Texas Instruments (1,000 employees), Freescale (200), Cypress Semiconductor (200), and National Semiconductor (80), as well as a host of fabless companies including Qualcomm and Nvidia. The range of activities at these centers is quite broad, and the training curve for domestically-educated engineers can be steep. In one instance we studied, a chip design project took twice as long to complete as planned.[118]

The oldest and largest of these centers is that of Texas Instruments (TI), which opened a software center in 1985. Most other U.S. investments in India have been made since the mid-1990s. The case of TI India, examined next, shows the potential for the other offshore chip design investments in India to develop over time.

Texas Instruments was the first semiconductor company to invest in India when it opened an office in Bangalore to work on its design automation software for internal use.[119] In 1988, the company added the design of mixed-signal (analog and digital combined) chips. In 1995, TI added design for DSP devices, the company's flagship product line. In 1998, TI India announced that it had taken its first DSP core from specification to working silicon over the preceding 2 years, and integrated a controller with the DSP function for the first time.

In 2003 TI India announced that it had created a highly integrated DSL chip that was the first to market to include significant analog elements on the same chip as the DSP and network processor. During the specification phase, a team of 20 engineers went to TI's Dallas

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[111] "Synopsys Teams with China's Ministry of Science and Technology, SMIC," Nikkei Electronics Asia, March 21, 2003; "An Uneven Playing Field," Electronic News, July 3, 2003; "China nurtures home-grown semiconductor industry," EBN, December 8, 2003; "China government to support Solomon Systech, Actions and Silan," DigiTimes, April 14, 2005.
[112] "China to form R&D fund to replace VAT rebate, says report," EE Times, April 15, 2005.
[113] Saxenian (2002).
[114] "Work begins on Hyderabad fab, doubt cast on IBM role," EE Times, June 27, 2005.
[115] Data from NASSCOM, India's IT industry trade group, in "Designed To Win." Business India, September 1, 2003.
[116] "India expands tech incubator initiative, seeks new investment," EE Times, August 12, 2004.
[117] "Intel, TSMC Set Up Camps In Developing Asian Markets," WSJ.com, August 30, 2002.
[118] E-mail communications with Indian chip designer, June 2005.
[119] The following description is based on a compilation of published accounts and the corporate web site.

headquarters and worked for 3 months with TI system engineers and dealt directly with TI customers about their requirements. The 130nm-linewidth, 13-million-transistor design was completed in India over the next year by a team of 70, worked the first time, and gave rise to eight patent applications for improvements to DSL technology. TI India had 225 U.S. patents as of August 2003.

TI India also develops design library elements, the basic building blocks needed for physical design, for TI's new processes. Although library elements are low-level intellectual property, they are critical inputs to the design process and used throughout TI's R&D infrastructure. Moreover, the designers engaged in library construction are gaining valuable experience with designing for leading-edge process technology.

Since 1999, TI India has won several awards from EDN Asia, a design industry publication, for its chips. In 2004, a very high-performance analog-to-digital converter was touted during an interview by the company's CEO, who mentioned in passing that it had been designed primarily in Bangalore.[120]

Texas Instruments is the pioneer among the large, vertically-integrated chip companies in terms of the in-house offshoring of chip design to India, but it is far from unique. The trade press regularly publishes announcements by other semiconductor companies of expansions of their Indian design centers., most of which were created in the 1990s. A fabless company we interviewed described how they started their Indian team in 2004 with logic design and will eventually expand it to doing complete derivative products.[121] A quarter of the company's 500-plus design engineers are now located in India.

We now turn to the thorny and complex question of the impact of the offshoring of chip design on the U.S. market for chip designers.

E. The job picture in the U.S.

The picture in the job market for U.S. chip designers is unclear, but the short-term dynamic of expansion overseas with modest growth of domestic design centers gives some cause for concern. However past experience in the semiconductor industry serves as a reminder to be cautious in extrapolating from the present.

During the past five years, the many forces affecting the semiconductor industry include the severe recession during 2001, the recovery that stalled in 2004, the large decline in venture funding for start-ups that is only beginning to pick up, changes in the number of H1-B visas, and a drop in foreign student applications to U.S. graduate engineering schools since 9-11. It is difficult to disentangle the effect of the business cycle from any underlying long-run trend in the offshoring of design jobs. This caveat should be borne in mind during the following analysis of the U.S. labor market for electronics engineers (EEs) using Bureau of Labor Statistics (BLS) data.

Ideal data would be specific to chip design engineers. However this level of occupation and industry classification are not available. Instead the data presented here are for EEs in all industries over the period 1999-2004 and at EE data in a broadly-defined semiconductor industry.

The most detailed level of EE occupational detail is "Electronics Engineers, Except Computer" (occupational classification 17-2072). In addition to chip designers, this category includes product-level system designers and engineers who develop non-chip components. Within this category, 12% were in the semiconductor industry (NAICS 3344, see below) in 2004. Another 13% were in electronics-related industries, and 29% in telecommunications. The rest are scattered throughout other industries. According to non-BLS semiconductor industry data for 2000-2004, 4-10% of EE new graduates go into the semiconductor industry.[122]

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[120] "Texas Instruments collects on split fab strategy bet," EE Times, May 17, 2004.

[121] Interview, December 2004.

[122] Data are from the annual SIA Semiconductor Workforce Strategy Committee Survey, referenced in "SIA Workforce Strategy Overview," op.cit.

TABLE 11: Employment and Earnings for U.S. Electronics Engineers, 1999-2004

	Total EE Employment	Mean annual EE earnings	Percentage change in EE employment	Percentage change in total nonfarm employment
May 2004	135,560	$77,450	3.29%	0.56%
Nov.2003	131,240	$74,800	4.14%	-0.08%
2002	126,020	$71,600	2.28%	-0.36%
2001	123,210	$69,710	-0.39%	-1.36%
2000	123,690	$66,490	15.78%	1.94%
1999	106,830	$63,410	--	--

Source: BLS Occupational Employment Statistics web site, www.bls.gov/oes/home.htm, accessed April 15, 2005.

Table 11 shows a relatively strong national demand for electronics engineers. The rapid buildup during the telecom and Internet bubble is clearly visible in the 16% growth for 2000, but after a small correction in 2001, the level continues rising significantly faster than total nonfarm employment. Mean annual earnings continued to rise throughout the period and were 16.5% higher in 2004 than in 2000, while the consumer price index for Urban Wage Earners increased 9.2% over the same period.

The BLS industry-specific data, based on the North American Industry Classification System (NAICS), are also imprecise for our purposes. Employment and wage data are available for "Semiconductor and Other Electronic Component Manufacturing" (NAICS four-digit level 3344), which includes relatively low-value components such as resistors and connectors. The most relevant subcategory, "Semiconductor and related device manufacturing" (NAICS 334413), accounted for 39% of employees (and 45% of non-production workers) in the 3344 category in 2003, but occupation-specific data are not available at this level of industry detail.[123]

The data in Table 12 from the broadly-defined semiconductor industry for the two occupations involved in chip design, electronic engineers and software engineers (applications and systems) show a strong, although more variable, labor market for the period 2002-2004, the only years publicly available. EEs earn less than the software engineers in the four-digit semiconductor industry, and systems software engineers experienced the fastest earnings growth during the two-year period. Applications software engineers experienced a dip in employment in 2004 after strong employment growth in 2003, and EEs experienced a dip in employment in 2003 followed by very strong employment growth in 2004. This is consistent with the peak in the national unemployment rate for electrical and electronics engineers to 6.2% in 2003, as it converged for the first time in 30 years with the general unemployment rate, before falling back in 2004 to a more typical rate of 2.2%.[124]

[123] U.S. Census Bureau, "Statistics for Industry Groups and Industries: 2003", Annual Survey of Manufactures, April 2005.

[124] Data were provided by Ron Hira. BLS redefined occupations beginning with the 2000 survey covering 1999, but there is no evidence that the redefinition has contributed to the post-bubble unemployment rise. See also "It's Cold Out There", IEEE Spectrum, July 2003.

TABLE 12: Employment and Earnings for U.S. Semiconductor Engineers, 2002-2004

	Total Employment	Mean Annual Earnings	Percentage change in employment	Percentage change in earnings
May 2004				
SoftwareApplications	7880	$83,060	-7.3%	+2.6%
SoftwareSytems	6070	$90,240	+7.1%	+6.4%
ElectronicEngineer	16,580	$78,350	+23.0%	+3.3%
May 2003				
SoftwareApplications	8500	$80,970	+13.9%	+2.9%
SoftwareSytems	5670	$84,790	+10.3%	+4.6%
ElectronicEngineer	13,480	$75,870	-1.5%	+4.4%
2002				
SoftwareApplications	7460	$78,710	--	--
SoftwareSytems	5140	$81,060	--	--
ElectronicEngineer	13,690	$72,680	--	--

Source: BLS Occupational Employment Statistics web site, www.bls.gov/oes/home.htm, NAICS 334400 occupations

Based on the available government data, the current wave of expansion of in-house offshore design centers and the growth of international design outsourcing does not appear to have had a major negative impact on the semiconductor labor market in the U.S. to date, but results from a regional survey reveal underlying strains. Silicon Valley, considered the cradle and creative font of the semiconductor industry, is experiencing a more difficult job climate. Silicon Valley jobs in the semiconductor industry declined 3.6% in 2004 (second quarter) compared to a year earlier, although semiconductor earnings, which averaged considerably above the national average at $120,000, rose 13.5% in 2003. Overall the number of jobs in the Silicon Valley has continued to decrease since 2001.[125]

The situation is also more difficult for older engineers, who face rapid skill obsolescence. We have heard in our research interviews that chip companies value new graduates, who are trained with the newest technology and command lower salaries. The 2004 salary survey by the EE Times found almost no difference in engineers' average salary at 40-44 years old ($104,000) versus 55-59 ($105,000).[126] Experienced design engineers are often forced to work on mature technologies, which pay less. For example, the EE Times survey found that the average annual salary for U. S. and European engineers skilled at designing for the latest chip process technology was $107,000, whereas engineers designing for the more mature analog technology averaged $87,000.[127]

Perhaps unsurprisingly, industry participants themselves are split on the significance of offshoring for the U.S. job market. A 2004 survey of more than 1,453 chip and board design engineers and managers by EE Times shows that about half saw foreign outsourcing as leading to a reduction in headcount. Qualitative opinions in the survey were also divided, with optimists noting that reduced costs made for a stronger company and a more secure job, while the

[125] Joint Venture: Silicon Valley Network, "2005 Index of Silicon Valley," available online at www.jointventure.org/PDF/JVIndex2005_FINAL.pdf. They use state unemployment insurance data, which is the basis for the Census data.
[126] "Mean wages edge closer to six-figure mark," EE Times, August 25, 2004.
[127] "After 10-year surge, salaries level off at $89k," EE Times, August 28, 2003.

pessimists bemoaned downward pressure on wages and employment plus a possible loss of intellectual property and, in the long run, industry leadership.[128]

We have observed some of the same dynamics of design job movement over the business cycle as occurred during the offshoring of assembly. A wave of design offshoring took place at the height of the dot.com bubble. When the cascading effect of the subsequent downturn reached the semiconductor industry, chip companies cut staff at home. Now that the recovery requires expansion of design operations, chip companies appear to be expanding design operations abroad faster than at home.[129] It is too early to predict where this relative shift in the geographic distribution of employment will find a new equilibrium.

V. Synthesis and conclusion

This section revisits the lessons from the earlier periods of offshoring of the semiconductor value chain in light of what is known so far about the offshoring of design before turning to a discussion of policy issues.

A. Assembly, fabrication, and design compared

The first lesson from the experience of assembly offshoring was that a partial move offshore to reduce costs can keep the industry competitive while allowing it time to adjust to a changing market environment. From the 1960s to the 1980s, the greatest source of anxiety was low-cost competition from Asia and a shift in importance from military to consumer electronics applications. Today, the offshoring of design is being driven by the rising fixed costs of chip design at a time when the industry's key application market is changing from the corporate computing sector to the price-sensitive consumer multimedia market. Offshoring appears to be a vital tool for allowing U.S. firms to bring complex chips to market at competitive prices and to expand the market for lower-cost chips in the developing countries.

A second lesson is that offshoring can lead to hollowing out, which was the case for U.S. chip assembly. As the example of Texas Instruments' 20-year old Indian design subsidiary, the work being done offshore will increasingly resemble that being done at home. Some start-ups have already adopted a structure featuring minimal high-level design staff in the U.S. with the bulk of engineering done in low-cost Asian locations. We expect the phenomenon of these virtual chip firms to become more widespread. Nevertheless, most, if not all, vital intellectual property will be developed and retained close to headquarters. Furthermore, we expect the large firms who employ large design groups in the U.S. to continue to do so. Therefore we do not anticipate a hollowing out of chip design comparable to what occurred with chip assembly.

The third lesson from the offshoring of assembly is that in-house offshoring can give rise to international outsourcing as local suppliers spring up alongside U.S. and other subsidiaries. It is far from clear that this will happen in chip design. Many of the founders of foreign start-ups have educational and work experience in the U.S. Foreign start-ups also benefit from policy interventions, as in China; from the strength of related activity, such as the Indian emergence of chip design on the back of the successful software industry; or some combination of the two, as in Taiwan. It seems probable that local companies will continue to spin off from U.S. subsidiaries to offer design services and reusable functional blocks. For the time being these lower-level design activities are mostly complements rather than competitors to U.S. firms.

Because design is more central to the firm than was assembly, the diffusion of design knowledge through in-house offshoring and international outsourcing might give rise to rivals that could ultimately threaten U.S. industry leadership and U.S. design jobs. The prospects vary greatly by the institutional environment in each location. As discussed above, Taiwan's fabless

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[128] "It's an outsourced world, EEs acknowledge," EE Times, August 27, 2004.

[129] See, for example, "The perfect storm brews offshore," Electronic Business, March 2004, accessible at www.reed-electronics.com/eb-mag/toc/03%2D01%2D2004/

sector, which did not arise as an outgrowth of U.S. design offshoring, is nearly a generation behind U.S. rivals in terms of innovative products. For now, local firms in India have generally avoided the fabless model, but in China there is a small but increasing number of fabless firms targeting world markets. Although for now Chinese firms lack experienced engineers and managers and are be behind Taiwan in their development of innovative products, this will gradually shift in the years ahead. It is too early to know where this process will end.

One of the observations from the offshoring of fabrication was that the offshoring of high-end activities in developed countries for market access was partially offset by cross-investments in the U.S. by European and Japanese firms. As discussed above, this is definitely the case for design, with the addition that such cross-investments may also be made in pursuit of specialized resources. Even ambitious small firms from relatively low-cost countries such as Taiwan are often compelled to invest in a small design center in Silicon Valley to access the expert skills available there. This has helped to blunt the effect of the in-house offshoring of chip design by U.S. firms.

The other lesson from the fabrication experience was that the development of the activity in new locations can lead to restructuring of the industry. In the case of fabrication, this meant that the emergence of chip foundries in Asia spurred the growth of the U.S.-dominated fabless sector. This was a long-term process, and it is too early to be sure if anything of this type will happen with design. The phenomenon of virtual chip firms, with most design and other activities offshore, may be spreading. This will remain true to the extent that it confers cost advantages over fabless rivals.

B. Policy issues

Offshoring appears to be a largely positive phenomenon at the industry level. The reduced costs and the flexibility provided by offshore design centers has allowed both new entrants and incumbents in the U.S. to maintain their competitive advantage despite the rising cost of the typical chip design. The lower costs have translated into growing consumer markets, both for advanced products in the developed countries and for scaled-down products in developing countries, especially fast-growing Asian markets. U.S. companies have also become savvy about how to develop products for regional markets, and often locate design and marketing activities accordingly. In addition, U.S. companies have carefully considered what intellectual property they must protect and keep close to home for strategic reasons, and what activities can be sent offshore, often with new protections in place.

The industry's offshoring has gone well beyond the point where blunt instruments such as trade policy can help engineers without harming companies. Taxes or quotas on traded activities or goods would raise the cost structure of the many companies who have already invested offshore whether they are designing primarily for the foreign or the domestic chip market.

Policy is thus unlikely to be able to improve the demand side of the labor market, and industry has been active in lobbying for changes on the supply side in the form of education and immigration changes. The Winter 2005 newsletter of the Semiconductor Industry Association includes articles such as "Maintaining Leadership As Global Competition Intensifies" by the organization's president and "America Must Choose To Compete" by the outgoing CEO of Intel. One of the main targets of these industry analyses is education. Higher education policies, which reflect both university decisions and government funding, determine the number and country of origin of engineering graduates at all levels.

The importance of foreign nationals in our MS and PhD programs in Electrical Engineering has a direct impact on the supply of engineers both in the United States as well as China and India. Foreign graduates of U.S. engineering schools must obtain temporary visas, usually H1-B visas for up to six years, before they can work in the U.S. after graduation. The complex issues relating to immigration and educational policies are controversial and a thorough

discussion of them is beyond the scope of this paper. Experts cannot even agree if the U.S. is educating too few engineers (and scientists) or is facing an engineer shortage.[130]

Government policies regulating immigration, especially the issuance of H1-B (Non-Immigrant Professional) and L-1 (Intra-Company Transfer) visas, have an important impact on the number of foreign engineers engaged in semiconductor work. Changes in the policy appear to have had an effect on in-house offshoring. When the number of H1-B visas issued was dramatically cut in 2002 and 2003 in response to the recession, many U.S. companies used the opportunity to send foreign nationals with U.S. education and experience back to India and China to help build operations there. Although the salaries are much lower, the purchasing power parity comparisons indicate that engineers still enjoy a high standard of living after returning home. For example, the PPP-adjusted salary of a design engineer is $77,300 in India and $69,400 in China, compared to $82,000 in the U.S.[131] Using data from 'PhDs…Ten Years Later' survey, a study of foreign-born U.S. PhDs in science and engineering shows the importance of personal values, work-related considerations, and formal and personal ties, as opposed to purely economic motivation, in the decision to return home.[132]

An area of policy that has received less attention is compensation to engineers who are harmed by offshoring. Thanks to the offshoring of chip design, consumers benefit from lower prices and new products (although much of that benefit is received outside the United States), but some of the short-term cost of the offshoring is borne by engineers in particular companies or industry sectors whose companies are restructuring globally. Currently, white-collar workers like chip designers don't qualify for trade-adjustment assistance from the government when their jobs are sent abroad. It would make sense to help these workers with retraining and other forms of assistance that will keep these highly-skilled individuals productive.

Finally, more and better data are needed. As researchers in other industries have noted, more labor market data, both for the U.S. and our trading partners, are needed in order to properly understand offshoring and its effects. National policies affecting education, labor markets, and innovation will continue to be based upon informed speculation.

The semiconductor industry is still in the early stages of a complex dynamic process, and policy interventions need to be flexible. At this point it is hard to say what the impact of design offshoring will be on the competitive position of the U.S. semiconductor industry, how long it will take for the economy to adjust, and whether the new equilibrium will be acceptable. What happens to the U.S. semiconductor industry and its workers has important consequences for the country, including the jobs created and the technology developed.

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[130] See, for example, National Research Council (2000), National Research Council (2001), Freeman (2003), Butz and others (2004), and Task Force On The Future Of American Innovation (2005).

[131] This calculation is based on the PPP of .194 for India and .216 for China reported in the Testimony for the IEEE by Ron Hira to the Small Business Committee, available at www.cspo.org/products/lectures/061803.pdf. The PPP adjustment is applied to the estimated $15,000 salaries for India and China reported in Table 10 of this paper.

[132] Gupta (2005).

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